Docket No. 500.39826CX1/E5828-04EU

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Seiichiro KANNO *et al.*
Serial No.	:	Unassigned (§53(b) Cont. of 09/799,527 filed 3/7/2001)
Filed	:	07 October 2003
For	:	SEMICONDUCTOR MANUFACTURING APPARATUS AND METHOD OF PROCESSING SEMICONDUCTOR WAFER USING PLASMA AND WAFER VOLTAGE PROBE
Art Unit	:	Unassigned (Parent - 1763)
Examiner	:	Unassigned (Parent - Ram N. Kackar)
Conf. No.	:	Unassigned (Parent - 4591)

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
POB 1450
Alexandria, Virginia 22313-1450

7 October 2003

Sir:

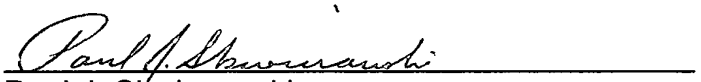
In the matter of the above-identified application, Applicant hereby submits the attached information for consideration by the Office under 37 C.F.R. §§1.97 and 1.98, as listed on the accompanying Form PTO-1449.

The present application is a continuation of Serial No. 09/799,527 filed 7 March 2003, pending. The information listed on the attached Form PTO-1449 was previously cited by or submitted to the Office in the prior application. Therefore, in accordance with 37 CFR §1.98(d), no copies of the listed references are required. Further, in accordance with 37 CFR §1.98(3)(i), a concise explanation of relevance or translation was submitted in the prior application for each item of information not in the English language, and as indicated in MPEP §609A(3), no separate concise

explanation of relevance is required because the relevance of the information does not differ from its relevance as explained in the prior application.

This Information Disclosure Statement is being filed concurrently with the above-identified application or within three (3) months of the filing date, and is therefore timely, and no Petition or fee is possible or required for this submission.

Respectfully submitted,



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Sheet 1 of 1

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO.	SERIAL NO.
		500.39826CX1	Unassigned
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		APPLICANT	
		Seiichiro KANNO *et al.*	
(Use several sheets if necessary)		FILING DATE	GROUP
		7 October 2003	Unassigned

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
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							Yes	No
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AU	Smith, CIRCUITS, DEVICES, AND SYSTEMS-A First Course in Electrical Engineering, 3RD Ed., John Wiley & Sons, Inc., 1973.
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Examiner	Date Considered